

Appl. No. 10/604,354  
Amtd. dated August 08, 2006  
Reply to Office action of May 19, 2006

**Amendments to the Claims:**

Claim 1 (currently amended). An electrostatic discharge protection circuit comprising:

an npn Darlington circuit comprising an input end and an output end; and  
an N-type channel metal-oxide semiconductor (NMOS) transistor, a drain of the  
5 NMOS transistor connected to the input end of the npn Darlington circuit, a  
source of the NMOS transistor connected to a control end of the npn Darlington  
circuit, a gate of the NMOS transistor connected to the output end of the npn  
Darlington circuit;

10 wherein the npn Darlington circuit further comprises two npn-type bipolar junction  
transistors (BJTs), each npn BJT comprising an N+ buried layer, a P well formed  
on the N+ buried layer, an N well formed on the N+ buried layer around the P  
well, and an N+ node formed in a top side of the P well; and the NMOS  
transistor comprises an N+ buried layer, a P well formed on the N+ buried layer,  
an N well formed on the N+ buried layer around the P well, and two N+ nodes  
15 formed in a top side of the P well;

the two BJTs and the NMOS transistor are formed on a P-substrate, and the N wells  
of the two npn BJTs and the NMOS transistor are used to isolate the P wells and  
the P-substrate; and

20 further comprising a P-epi layer formed on the P-substrate, and wherein the N wells  
of the two npn BJTs and the NMOS transistor are formed on the P-epi layer.

Claims 2-5 (cancelled).

25 Claim 6 (currently amended). The electrostatic discharge protection circuit of claim 1  
claim 3 wherein the circuit is manufactured by a BiCMOS process.

Claim 7 (original). The electrostatic discharge protection circuit of claim 1 wherein the  
npn Darlington circuit further comprises two npn BJTs, each npn BJT

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comprising a deep N well, a P well formed on the deep N well, and an N+ node formed in a top side of the P well; and the NMOS transistor comprises a deep N well, a P well formed on the N well, and two N+ nodes formed in a top side of the P well.

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Claim 8 (original). The electrostatic discharge protection circuit of claim 7 wherein the two BJTs and the NMOS transistor are formed on a P-substrate, and the deep N wells of the two npn BJTs and the NMOS transistor are used to isolate the P wells and the P-substrate.

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Claim 9 (original). The electrostatic discharge protection circuit of claim 8 wherein the circuit is manufactured by a CMOS process.

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Claim 10 (original). The electrostatic discharge protection circuit of claim 1 wherein the input end of the npn Darlington circuit is connected to an input end of another circuit.

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Claim 11 (original). The electrostatic discharge protection circuit of claim 1 wherein the input end of the npn Darlington circuit is connected to a voltage source.

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Claim 12 (original). The electrostatic discharge protection circuit of claim 1 further comprising:

a pnp Darlington circuit, an input end of the pnp Darlington circuit connected to the input end of the npn Darlington circuit, an output end of the pnp Darlington circuit connected to a voltage source; and

a P-type channel metal-oxide semiconductor (PMOS) transistor, a drain of the PMOS transistor connected to the input end of the pnp Darlington circuit, a source of the PMOS transistor connected to a control end of the pnp

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Darlington circuit, a gate of the PMOS transistor connected to the output end of the pnp Darlington circuit.

Claim 13 (cancelled).

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Claim 14 (new). An electrostatic discharge protection circuit comprising:

an npn Darlington circuit comprising an input end and an output end; and  
an N-type channel metal-oxide semiconductor (NMOS) transistor, a drain of the NMOS transistor connected to the input end of the npn Darlington circuit, a  
10 source of the NMOS transistor connected to a control end of the npn Darlington circuit, a gate of the NMOS transistor connected to the output end of the npn Darlington circuit;

wherein the npn Darlington circuit further comprises two npn-type bipolar junction transistors (BJTs), each npn BJT comprising an N+ buried layer, a P well formed  
15 on the N+ buried layer, an N well formed on the N+ buried layer around the P well, and an N+ node formed in a top side of the P well; and the NMOS transistor comprises an N+ buried layer, a P well formed on the N+ buried layer, an N well formed on the N+ buried layer around the P well, and two N+ nodes formed in a top side of the P well;

20 the two BJTs and the NMOS transistor are formed on a P-substrate, and the N wells of the two npn BJTs and the NMOS transistor are used to isolate the P wells and the P-substrate; and

further comprising an N-epi layer formed on the P-substrate, and the N wells of the two npn BJTs and the NMOS transistor are formed on the N-epi layer.

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Claim 15 (new). The electrostatic discharge protection circuit of claim 14 wherein the circuit is manufactured by a BiCMOS process.

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5 Claim 16 (new). The electrostatic discharge protection circuit of claim 14 wherein the npn Darlington circuit further comprises two npn BJTs, each npn BJT comprising a deep N well, a P well formed on the deep N well, and an N+ node formed in a top side of the P well; and the NMOS transistor comprises a deep N well, a P well formed on the N well, and two N+ nodes formed in a top side of the P well.

10 Claim 17 (new). The electrostatic discharge protection circuit of claim 16 wherein the two BJTs and the NMOS transistor are formed on a P-substrate, and the deep N wells of the two npn BJTs and the NMOS transistor are used to isolate the P wells and the P-substrate.

15 Claim 18 (new). The electrostatic discharge protection circuit of claim 17 wherein the circuit is manufactured by a CMOS process.

Claim 19 (new). The electrostatic discharge protection circuit of claim 14 wherein the input end of the npn Darlington circuit is connected to an input end of another circuit.

20 Claim 20 (new). The electrostatic discharge protection circuit of claim 14 wherein the input end of the npn Darlington circuit is connected to a voltage source.

25 Claim 21 (new). The electrostatic discharge protection circuit of claim 14 further comprising:  
a pnp Darlington circuit, an input end of the pnp Darlington circuit connected to the input end of the npn Darlington circuit, an output end of the pnp Darlington circuit connected to a voltage source; and  
a P-type channel metal-oxide semiconductor (PMOS) transistor, a drain of the

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PMOS transistor connected to the input end of the pnp Darlington circuit, a source of the PMOS transistor connected to a control end of the pnp Darlington circuit, a gate of the PMOS transistor connected to the output end of the pnp Darlington circuit.

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